**DAILY ASSESSMENT FORMAT**

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| **Date:** | **28 MAY 2020** | **Name:** | **VAISHNAVI M** |
| **Course:** | **LOGIC DESIGN** | **USN:** | **4AL18EC055** |
| **Topic:** | **1.ANALYSIS OF CLOCKED SEQUENTIAL CIRCUITS**  **2.DIGITAL CLOCK DESIGN** | **Semester & Section:** | **IV SEM & A SECTION** |
| **GitHub Repository:** | **vaishnavi-manjunath** |  |  |

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| **FORENOON SESSION DETAILS** | | |
| **Image of session** | | |
| **Report – Report can be typed or hand written for up to two pages.**  In this module we learnt:  **SIMULATION OF CIRCUIT:**   * **D- FLIP FLOP** | | |
|  |  |  |  |
| **Date:28 MAY 2020** |  | **Name: VAISHNAVI M** |  |
| **Course: PYHTHON** |  | **USN: 4AL18EC055** |  |
| **Topic: OBJECT ORIENTED PROGRAMMING** |  | **Semester & Section: IV SEM & A SECTION** |  |
| **AFTERNOON SESSION DETAILS** | | |
| **Image of session** | | |
| **Report – Report can be typed or hand written for up to two pages.**  **TOPICS LEARNT:** | | |